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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Bullis, et al.

Serial No: 09/409,940 Group Art Unit: 2123

Filed: September 30, 1999 Examiner: Ferris III, F.

For: METHOD AND SYSTEM FOR PROVIDING HIERARCHICAL SELF-CHECKING IN ASIC SIMULATION

Commissioner for Patents
P.O. Box 1450
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MPEP 2164

DECLARATION UNDER 37 C.F.R. 1.132

I, Raj Singh, hereby declare that:

1. I am the inventor of the subject matter recited in the claims of the above-identified application.

2. I have reviewed the specification of the present application.

3. It is my opinion that one of ordinary skill in the art will readily understand that the method and system in accordance with the present invention, as disclosed in the present application, are based on inter-process communication between the units under test (islands), embodiments of the system and method in accordance with the present case (snooper, checker, and generator) and the test case. The islands reside in the test bench during use of the snooper, checker, and generator.

4. It is my opinion that based upon reading the specification of the present application, one of ordinary skill in the art would readily realize that each snooper, checker and generator can be considered to include a physical portion and a logical portion, which is termed the

intelligence in the specification. The physical portion includes interfaces and a mechanism for controlling the interfaces. The interfaces of the snooper, checker, and generator couple to the interface(s) of the island. It is my opinion that one of ordinary skill in the art would readily recognize that the interfaces typically include I/O ports for connecting to the island and a process for controlling the I/O ports that operates in system-clock domain where simulation time is advanced.

5. As described in the specification, the intelligence of the snooper, checker and generator can be implemented using a number of languages. In one embodiment, the intelligence of the snooper, checker and generator function as follows. As described in the specification, the test case provides data and a framework for the generator. The test case thus requests the generator to perform a particular simulation of the island and provides data for the simulation. It is my opinion that one of ordinary skill in the art will readily recognize that in requesting that the generator perform a particular simulation, the test case calls functions provided by, or procedures contained in, the intelligence of the generator. Thus, the intelligence required in the test case is minimal. It is also my opinion that one of ordinary skill in the art will also recognize that the intelligence of the generator helps carry out the desired procedures called by the test case, including providing the appropriate and preferably randomized inputs to the island in response to a request for service from the test case. The intelligence of the generator also uses the data provided by the test case to generate these inputs.

6. The intelligence of the snooper and checker preferably causes the snooper and checker to wait in loops for outputs to be provided from the island. The intelligence of the snooper and checker also obtain the outputs from the interfaces (the physical portion) and check

the outputs against desired outputs. As described in the specification, the intelligence of the checker can also generate the desired outputs.

7. Thus, the intelligence of the snooper, checker and generator can be viewed as providing internal data structure (buffering and queuing) and a process for manipulating these data structures in response to service request by other snooper, checker and generator combinations and test case(s) via a set of procedure calls and global signals. The physical and logical parts of each snooper, checker and generator communicate with each other via a set of internal signals. In one embodiment, the logical part operates in simulator's delta-time domain.

8. One embodiment of the method and system in accordance with present invention as recited in varying scope in the claims of the present application was successfully applied in design of a Common ATM Data mover (CAD) processor chip. Other embodiments of the method and system in accordance with the present invention have been since applied in several other ASIC designs. Consequently, the snooper, checker and generator can be used in developing a variety of ASICs.

9. Thus, upon reading the specification, it is my opinion that one of ordinary skill in the art will enable one of ordinary skill in the art to make and/or use the snooper, checker, and generator described in the specification and recited in the claims of the application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States

Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Raj Singh

5/14/2003

Date